استخدام اسلوبى التردد والتقطيع العرضى للنبضة لتصميم متحكمات فى حمل يغذى من منظومة خلايا شمسية

Using of Frequency and Pulse Width Modulation Techniques to Design Load Controllers Supplied by Solar Cells Array

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فى هذا البحث يتم تصميم متحكم فى حمل موصل بنظام فوتوفولتى. ويوضع المتحكم بين عنصر التخزين (بطارية حامضية) والحمل. يتم تصميم المتحكم باسلوبين هما اسلوبى التردد والتقطيع العرضى للنبضة. يتم وصف دقيق لخطوات التصميم للمتحكمات المقترحة ويتم ايضا تحديد الاداء الكهربى للمتحكمين المقترحين عمليا.

Abstract

The aim of this paper is to design a load controller coupled with a photovoltaic power system. The controller interfaces between the energy storage element (lead acid battery) and the load. The controller is designed using two techniques, the frequency and pulse width modulation technique. The design procedure of the proposed controller using each technique is briefly illustrated. The electrical behavior of each controller is experimentally investigated.

Introduction

Recently, conversion of solar energy directly into electricity for domestic applications using arrays of photovoltaic cells is gaining increasing attention [1-2]. Consequently, the design and operation of the controllers connected with loads supplied from photovoltaic systems are very important. Reference [3] describes the application of load control using frequency and voltage sensing device. This paper presents two techniques for controlling the output voltage of the lead acid battery supplied by solar cells array. The first technique used is applied by changing the triggering pulse frequency of a power switch. The second one is designed using the pulse with modulation technique. It is applied for controlling the battery output voltage, and hence controlling the load, by changing the pulse duty cycle. The proposed design procedure of each controller is carried out. The electrical performance of the designed controllers are experimentally investigated.

Controller Techniques

The techniques, which are used in the design of the controller, are.

1- The frequency technique.
2- The pulse width modulation technique.

(1) Control using Frequency Technique:

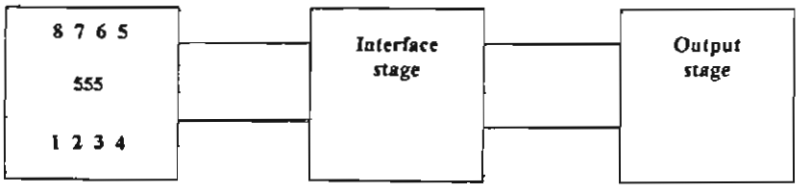

Fig. 1 Block Diagram of the Frequency Technique Load Controller

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The proposed frequency technique load controller consists of three main circuits. The first circuit is an oscillator, which is designed as an astable multivibrator. The second circuit is the interface stage, which connects between the oscillator output and the output stage. The interface stage is a very important stage because the output stage (power transistor) must be provided with a very large current than the oscillator output. The base of the power transistor is supplied by a current of few amperes on the other hand, the oscillator output supplies only few milliamperes so, as a result of connecting the output stage directly to the oscillator, the multivibrator will be destroyed. The interfacing stage is designed as a normally off signal transistor circuit which operates as an inverter. This circuit must be designed accurately, and the transistor specifications are obtained from its data. The output stage is considered as a power transistor circuit. The base resistance R_{B1} of the power transistor must be designed accurately, its value depends upon the load current.

Controller Circuits Design

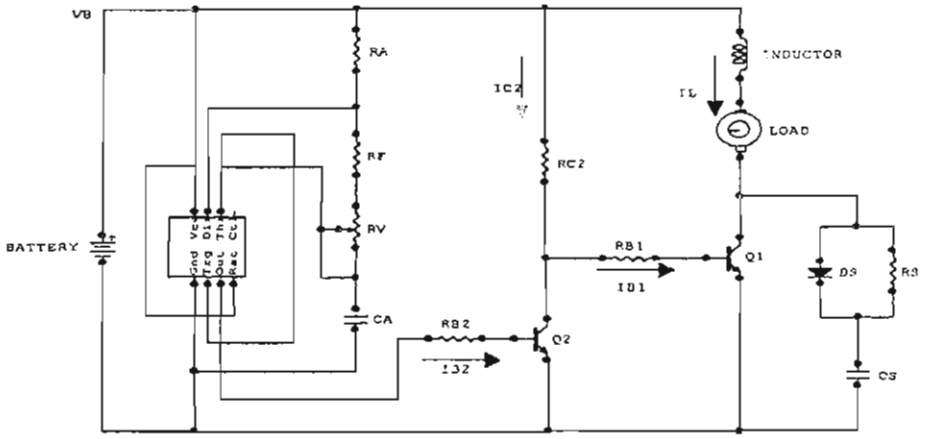

Fig. 2 Schematic Diagram of the Proposed Variable Frequency Controller

The design of this controller is initiated from the load, the rated value of the load current must be initially considered, this value is taken as a saturation current of the power transistor Q_1. The power transistor must operate in its saturation region; to make sure that most of the battery voltage is on the load. Hence, the voltage between Q_1 collector and emitter is equal to its saturation value (VCEsat), this value of voltage is very small and obtained from the transistor data sheet. Then, from transistor Q_1 data sheet, the value of h_{Femin1}, is determined. The h_{Femin1}, parameter is defined as,

$$h_{FEmin1} = I_{Csat1} / I_{Bmin1} \quad (1)$$

Where:

I_{Csat1}: is the saturation current of the transistor Q_1, which is equal to the load current and I_{Bmin1} is the minimum current which must flow into transistor base to obtain a finite value of collector current. So,

$$I_{Bmin1} = I_{Csat1} / h_{FEmin1} \quad (2)$$

The next step of the design procedure is the selection of the saturation current of the signal transistor Q_2 (I_{Csat}) . This current is selected according to the following condition:

$I_{Csat2} >> I_{Bmin2}$ Hence ,

$$R_{C2} = (V_B - V_{Cesat2}) / I_{Csat2} \quad (3)$$

Where:

V_B: is the battery voltage, V_{CEsat2} is the saturation voltage of transistor Q_2, and it is determined from Q_2 data sheet, and I_{Csat2} is the saturation current of the signal transistor Q_2.

After that the value of R_{B1} is accurately designed. The design value of this resistance is determined at the instant when Q_1 becomes on. Hence, as Q_1 is in on state:

$$V_{BE1} = V_{BE1on}$$

The value of V_{BE1on} is determined from transistor Q_1 data sheet, and is equal to 0.7 volt. So, when Q_1 becomes on, Q_2 is in off state;

$$V_B = I_{Bmin1} (R_{C2} + R_{B1}) + V_{BE1on} \quad (4)$$

Hence ;

$$R_{B1} = (V_B - V_{BE1on} - I_{Bmin1} R_{C2}) / I_{Bmin1} \quad (5)$$

Selection of Transistor Q_2

Transistor Q_2 may be used as a power or a signal transistor. It's selected as a power transistor when its base current value has a few amperes. On the other hand, it is selected as a signal transistor, when the previous current has few millampers. When the value of I_{Csat2} is defined , then from Q_2 data sheet h_{FEmin2} is determined , So ;

$$I_{Bmin2} = I_{csat2} / h_{FEmin2} \quad (6)$$

This value of current is in millamperes. So , transistor Q_2 is taken as a signal one. The value of I_{Bmin2} must be equal or less than the rated output current of the I_{C555} used. Otherwise, another interface stage will be coupled with the collector circuit of the transistor. The base resistance R_{B2} coupled with the transistor is determined when Q_2 becomes on . Hence;

$$Vo = I_{Bmin2} R_{B2} + V_{BE2on} \quad (7)$$

Where :

Vo : is the I_{C555} output voltage, and its value is near to the battery voltage, V_{BE2on} : is determined from transistor Q_2 data sheet , and is taken as 0.7 volts .

$$R_{B2} = (Vo - V_{BE2on}) / I_{Bmin2} \quad (8)$$

Design of the Oscillator

The purpose of the oscillator design is to obtain definite pulses with different frequency value. The frequency range of the designed oscillator is up to 1 KHz. The oscillator circuit is designed as follows;

Initially, resistors R_A and R_F, shown in Fig. 2, are selected with fixed values equal to 1KΩ. Then , select capacitor C_A as you can, the best selection is a 0.1 μF. The selection of the variable resistor R_V depends upon the limits of the required frequency. At the instant of employing the whole value of the variable resistor R_V , the time of charging and discharging capacitor C_A are obtained by the following equations;

$$t_1 = 0.693 (R_A + R_F + R_V) C_A \quad (9)$$

$$t_2 = 0.693 (R_F + R_V) C_A \quad (10)$$

where : t_1, and t_2 are the capacitor charging and discharging time respectively.

The upper and the lower values of the selected frequencies are f_{min} and f_{max} . The value of f_{max} is obtained when only resistors R_A and R_F are inserted in the astable multivibrator circuit , then ;

$$t_{1min} = 0.693 (R_A + R_F) C_A \quad (11)$$

$$t_{2min} = 0.693 R_F C_A \quad (12)$$

$$F_{max} = 1/ (t_{1min} + t_{2min}) \quad (13)$$

$$F_{max} = 1 / (0.693 (R_A + 2R_F) C_A) \quad Hz \quad (14)$$

As the variable resistor R_V is inserted completely in the multivibrator circuit, the frequency slows down to a value of f_{min} then ;

$$t_{1max} = 0.693 (R_A + R_F + R_V) C_A \quad (15)$$

$$t_{2max} = 0.693 (R_F + R_V) C_A \quad (16)$$

Consequently ;

$$F_{min} = 1/(t_{1max} + t_{2max}) \quad (17)$$

So ;

$$F_{min} = 1/ (0.693 [R_A + 2 (R_F + R_V)] C_A) \quad (18)$$

As the astable multivibrator is designed, the design procedure of the variable frequency controller is completed.

Frequency Controller Under Design

The frequency controller under design operates in the range of :

$$5Hz \leq F \leq 1\ KHz$$

Now select the values of resistor R_A not less than 1KΩ and this value is fixed in the controller under design. From equation (14) , R_F is determined as $C_A = 0.1\ \mu F$ the designed value of R_F is 6715 Ω. From equation (18) , the value of designed resistor R_V is determined , which is equal to1436 KΩ. The designed value of R_{B1} is obtained as the load current is defined. The load under test is supplied by 1.7 ampere. Hence, select $I_{Csat1} = 1.7$ Ampere .From Q_1 data sheet, $h_{FEmin1} = 20$, consequently;

$I_{Bmin1} = 1.7 / 20 = 85$ mA .

after that, select $I_{Csat2} >> I_{Bmin1}$

Throughout the design of the controller , the selection of 0.1 Ampere for I_{Csat2} is very suitable. The value of R_{C2} is determined from equation (3) which is 114 Ω as $V_{CEsat2} = 0.6$ volt. The value of R_{B1} is obtained from equation (5) which is 17.76 Ω as $V_{BE1on} = 0.8$ volt. The value of R_{B2} is obtained from equation (8) which is 27KΩ as $V_{BE2on} = 0.8$ volt from its data sheet. A small inductance must be connected with the load for the protection purpose against the effect of (di / dt) . On the other hand , a snubber circuit of R_S , D_S and C_S elements must be connected across the collector emitter of Q_1 power transistor to protect it against the effect of (dv / dt). Suitable values of snubber circuit elements are taken as follows;

$R_2 = 100\ \Omega$ and $C_S = 47\ \mu F$

The power dissipation in each resistor must be taken into consideration in the design of each resistor.

Operation of the variable Frequency Controller

The testing of the designed variable frequency controller is carried out by inserting it into the circuit shown in Fig (3). The experimental test of the designed controller is carried out by measuring the following parameters ;

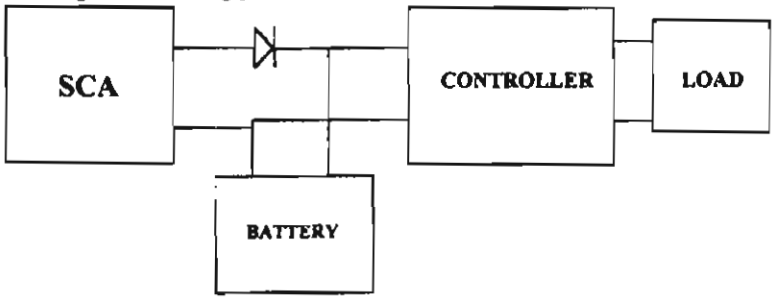

Fig 3 Connection Diagram of the Experimental Test Circuit.

F , V_{BE1} , V_{BE2} , V_{CE1} , V_B , V_C , I_{B1} , I_{B2} and I_L.

Where :

F is the frequency which change over a wide range of 5 Hz to 1000 Hz, V_{BE1} is the base emitter voltage of the power transistor, V_{BE2} is the base emitter voltage of the signal transistor, V_{CE1} is the collector emitter voltage of power transistor, V_{CE2} is the collector emitter voltage of the signal transistor, V_B is the battery voltage which is taken as a biasing voltage of the whole electronic circuits used, V_L is the load voltage which is equal to $V_B - V_{CE1}$, I_{B1} is the current flow to the base of the signal transistor, and I_L is the load current which is equal to the collector current of the power transistor. The electrical behavior of the designed controller is carried out by representing graphically all the previous parameters.

Behavior of the Power Transistor Circuit

The relation between the base current flows in the base of power transistor against frequency of the oscillator is shown in Fig 4 the figure shows that at very low frequency , 19 Hz , the base of the transistor is supplied by a very high current. conversely, at the high levels of frequencies the current takes a stable value less than that at low levels of frequencies. This is due to that at low frequencies the on time of the transistor is very high. so , the average value of the load current becomes very high and hence , the base current must be increased . Fig. 5 shows that the base emitter voltage of the power transistor against frequency takes a behavior similar to that in Fig. 4 also at low frequencies, the value of this voltage goes up rapidly. Where at high frequency it goes down and takes a stable value. The relation between the load voltage against frequency takes also the same behavior as in Figs 4,5. These behaviors assures that a small inductance must be connected with a pure resistive load. The inductance is used for damping the current generated at the initial of the operation as shown in Fig. 6.

Performance of Interface Transistor

The performance of the interfacing transistor is recorded experimentally by measuring some parameters which are the base current, and the base emitter voltage. The frequency is changed in a wide range from zero to 1000 Hz. Fig 7 illustrates the relationship between the base current drived into the base of the transistor and the pulse frequency. The current at low frequency has a very large value and decreases to a low value at large levels of frequencies . The relation between the base emitter voltage of the transistor and frequency is shown in Fig. 8 . It takes a behavior similar to that in Fig. 7. The lead acid battery is considered as the source of power for all controller elements . Fig. 9 shows the relation between the battery voltage and the pulse frequency. It shows that the battery reaches to a very low level at low frequency. This is due to that the controller element draw a very high current from the battery at this condition . conversely at high levels of frequencies, the controller element as well as the load draw low current from the battery. Hence, the battery voltage increases and reaches to a stable state as shown in Fig. 9. Fig. 10 represents the relation between the load current and the pulse frequency. The figure reveals that the designed controller has a narrow range of frequency for control approximately for about 19 Hz.

Pulse Width Modulation Controller

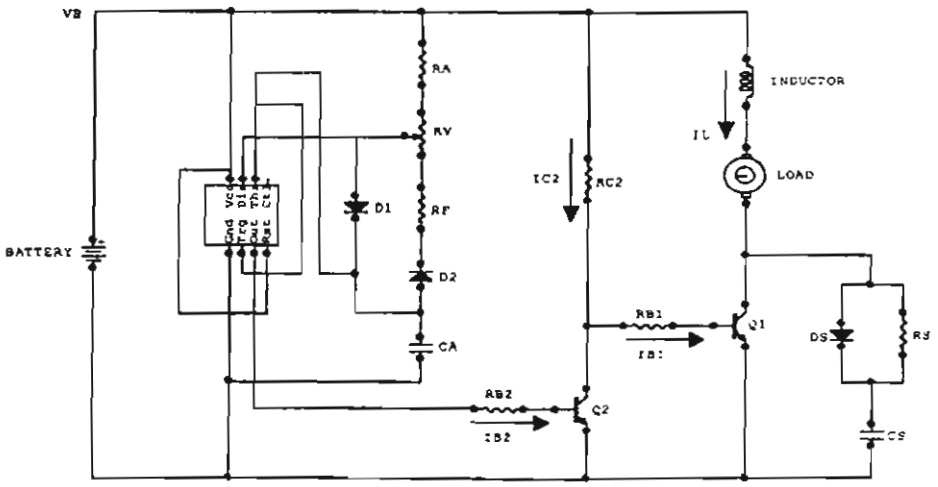

Fig. 11 Circuit Diagram of the Pulse Width Modulation Controller

Pulse width modulation technique depends upon the change of the duty cycle while the pulse frequency remains constant. By changing the variable resistor R_v, a change of charging and discharging time of capacitor C_A may be occur. As the summation of charging and discharging resistance is constant during the test, the pulse repetition frequency becomes constant all the time. Diode D_1 becomes forward bias during the charging condition of C_A. On the other hand, diode D_2 becomes forward bias during the discharging of C_A. Fig. 11 represents the circuit diagram of the controller which employs the pulse width modulation technique. In the last situation of the frequency controller, an interface stage and output stage are coupled together with the oscillator circuit. The design procedures of the interface stage and the output stage are similar to that in frequency controller. The design procedures of the astable multivibator coupled with this controller are as follows:

The first step of the design procedure is to select the operating frequency (F) in (Hz). Then, select the minimum and maximum levels of the employed duty cycles. After that, take a condition when the variable resistor $R_V = 0$ so,

$$t_1 = 0.693 \quad R_A + CA \tag{19}$$

$$t_2 = 0.693 \, (R_F + R_V) \, C_A \tag{20}$$

Where:

t_1 is the charging capacitor time, and t_2 is the discharging capacitor time.

As the duty cycle (Dc) is at its minimum value so,

$$Dc = t_1 / (t_1 + t_2) \tag{21}$$

$$t_1 + t_2 = 1/F \tag{22}$$

Where:

F is the pulse repetition frequency.

Throughout the design, the value of capacitor C_A is selected with a suitable value. After that, R_A and R_F will be determined at the selected situation of Dc. The insertion Of the whole value of the variable resistance, means that the duty cycles reaches to its maximum. So,

$$t_1' = 0.693 \, (R1 + RV) \, CA$$

$$t_2' = 0.693 \, (R4) \, CA \tag{24}$$

And as the duty cycle becomes maximum;

$$Dc_{max} = t_1' / (t_1' + t_2') = t_1' / T \tag{25}$$

$$Dc_{max} = F \, t_1' \tag{26}$$

Where :

t_1' is the capacitor charging time at the condition of maximum duty cycle and t_2' is the capacitor discharging time.

The oscillator of the controller under design is designed as follows:

Select the minimum duty cycle as 5 %, and its maximum as 95 %. The pulse repetition frequency is selected as 200 Hz. Then, at minimum and maximum values of duty cycle R_A and R_B are determined. The summation of R_A and R_B for each case takes the same value.

Experimental Behavior of the Pulse Width Modulation Controller

The Experimental results of the operation of the pulse width modulation controller are represented throughout a family of figures. Fig. 12 illustrates approximately a linear characteristic of the base current of the power transistor against the duty cycle of the oscillator pulse. Fig. 13 show the relation between base emitter voltages of the power transistor Q_1 against the duty cycle. The figure represents also a linear characteristic as the previous figure. Fig 14 shows that at low duty cycle the interface transistor Q_2 requires high current for turning it on. On the other hand low current supplies it at high duty cycle to turn it on. The previous figures show that the power transistor takes the opposite behaviors than interface transistor. This due to that at the instant when the interface transistor is in on condition, the power transistor is in off state. Fig 16 gives the relation between the battery voltages against duty cycle. The voltage is inversely proportional with the duty cycle; it decreases as the duty cycle increases. This is due to

that the controller elements draw high currents at low levels of duty cycle and draw low current at high levels of the duty cycle. Fig 17 illustrates the relation between the load voltages against duty cycle; this voltage is directly proportional with the duty cycle. This is due to that the load is connected with the power transistor collector So, it takes a behavior as power transistor behavior. The load current against duty cycle is represented in Fig. 18, which takes similar characteristic as in Fig. 17. Fig. 18 reveals that the load control by using this controller is very suitable. This due that the control will be linear on the whole range of the duty cycle. On the other hand, the frequency controller has poor characteristics because the control using these types of controller gives the best control in a narrow range of frequency.

Conclusions

This paper presents a method for designing a load controller by using two techniques, variable frequency technique and pulse width modulation technique. The electrical behavior of the variable frequency controller shows that there is no control at high levels of frequency. On the other hand, a good control is obtained at low levels of frequency. This leads to that, this controller is not suitable for lighting load, but it is more suitable for a dynamic load, such as DC motors. The controller gives a good performance at different levels of insolation levels. The electrical behavior of the second designed controller gives a good performance with different loads. It has a good control at low values of duty cycles as well as at high values of it. The paper gives the accurate design procedures of the two controllers.

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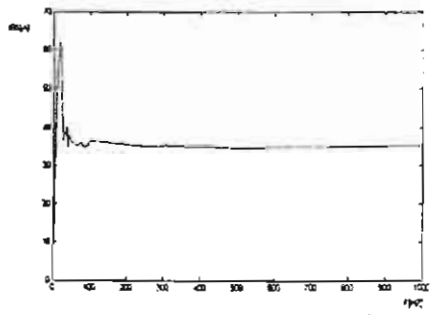

Fig. 4 Base current of power transistor against frequency

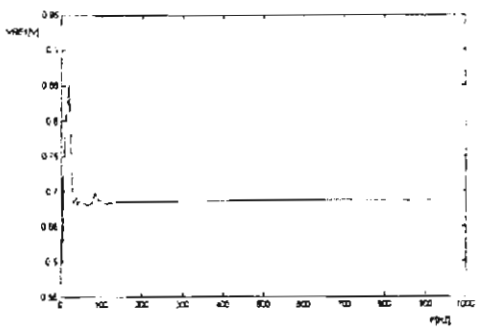

Fig. 5 Base emitter voltage of power transistor against frequency

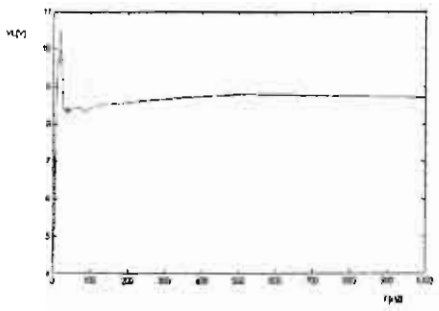

Fig. 6 Load voltage against frequency

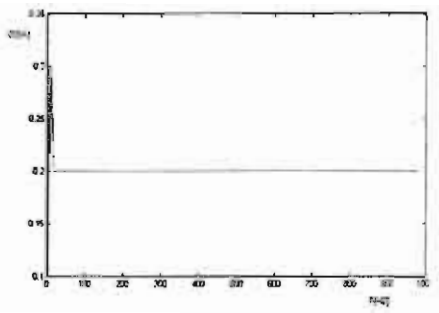

Fig. 7 Base current of signal transistor Q_2 against frequency

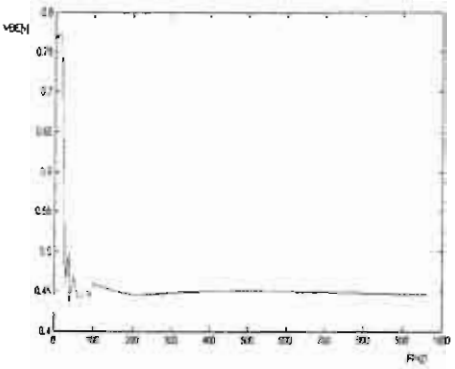

Fig. 8 Base emitter voltage of signal transistor against frequency

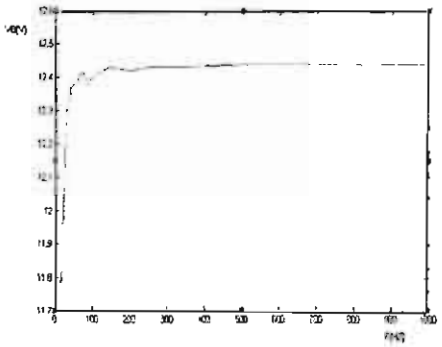

Fig. 9 Battery voltage against frequency

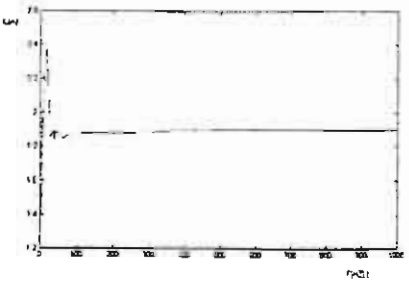

Fig. 10 Load current against frequency

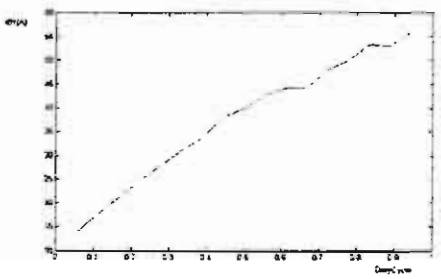

Fig. 12 Base current of power transistor against duty cycle

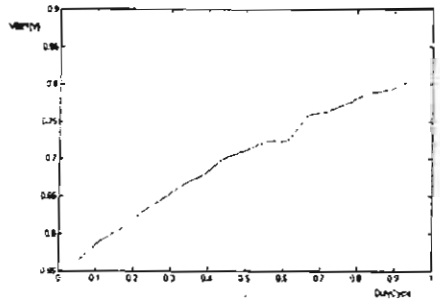

Fig. 13 Base emitter voltage of power transistor against duty cycle

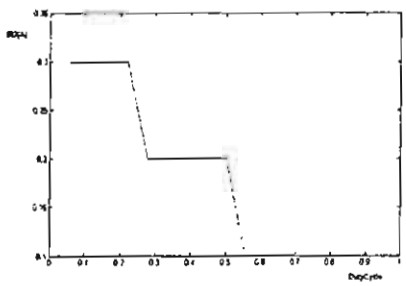

Fig. 14 Base current of signal transistor against duty cycle

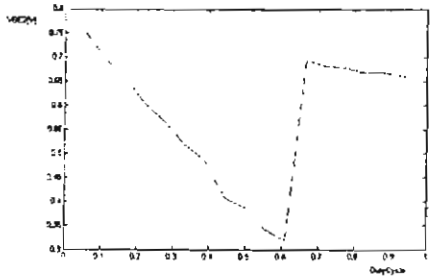

Fig. 15 Base emitter voltage of power transistor against duty cycle

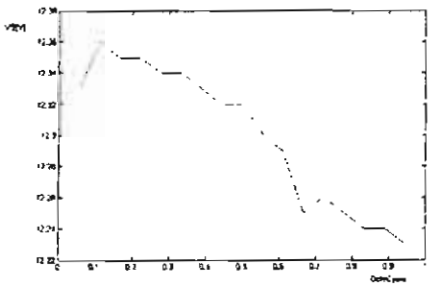

Fig. 16 Battery voltage against duty cycle

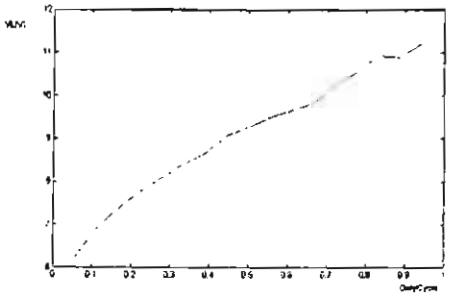

Fig. 17 Load voltage against duty cycle

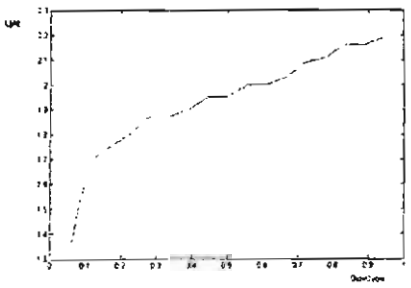

Fig. 18 Load current against duty cycle