أول (١٣)

University	:	*Menoufia*		*Date*	: *June 2019*
Faculty	:	*Electronic Engineering*		*Time*	: *90 Minutes*
Department	:	*Electronics and Communications Engineering*		*No. of pages*	: *1*
Academic level	:	*First Year*		*Full Mark*	: *35 Marks*
Course Name	:	*Electronics (2)*		*Exam*	: *Final Exam*
Course Code	:	*ECE 123*		*Examiner*	: *Assoc. Prof. Ahmed Nabih Zaki Rashed*

جامعة المنوفية

Question1: Complete the following sentences with the correct answer: (15 Marks)

i) JFET is abbreviation to....., while MOSFET is abbreviation to .....

ii) A major advantages of FET transistors are....., ...

iii) A FET is a .....controlled device.

iv) The basic terminals of FET transistors are ....., ..., and .....

v) The main difference between depletion mode and enhancement mode in FET transistor is .....

vi) V_P in FET transistor is called by ....., where the basic types of biasing in FET transistor are....., ..., ...and .....

vii) Forward transconductance (g_m) is rate of change of .....to the rate of change of .....when .....is constant.

Question 2: (20 Marks)

a) The 2N5459 JFET has typically I_{DSS}=9 mA, $V_{GS(OFF)}$=–8 V (maximum). Using these values, determine the drain current for V_{GS}=0 V, –1 V, and –4 V.

b) Voltage divider N channel enhancement MOSFET common source amplifier. Sketch the basic amplifier circuit diagram, sketch the small signal equivalent circuit and then find overall voltage gain. Sketch the output waveform for this circuit.

c) JFET with voltage divider bias circuit has the following parameters: V_{DD}=12 V, R_D=3.3 KΩ, R_S=2.2 KΩ, R_1=6.8 MΩ, R_2=1 MΩ, and V_D=7 V. Sketch the schematic view of the circuit. Estimate the gate voltage, the drain current, gate to source voltage and drain to source voltage.

مع تمنياتي لكم بالنجاح والتوفيق

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